REMARKS

Reconsideration and allowance of the above-identified application in consideration of the following supportive discussion/rebuttal arguments is respectfully requested.

Claims 1-2 and 5-6 were again rejected over the same combination of references. That is, claims 1-2 and 5-6 were rejected under 35 U.S.C. §103(a), allegedly, as being unpatentable over the combination of Yamazaki et al (USP 5,933,205) and Shimizu et al (USP 5,466,481) in view of Hasegawa (USP 5,064,779) and further in view of Takehashi et al (USP 5,712,496) or Ipri (USP 4,597,160). It is submitted, the invention defined in these claims could not have been achievable from the combined teachings of these references, including in the manner applied in the rejection. The following supportive discussion/rebuttal arguments, it is submitted, clearly shows this to be the case. This rejection is therefore traversed and withdrawal of the same is respectfully submitted.

One of the key aspects of the LCD device according to each of the independent claims 1 and 5 is that *variations of positions of peaks of depth distributions of concentration of impurities introduced into the polycrystalline silicon semiconductor layer, crystallized by laser annealing, by implantation to determine a conductivity type thereof are within 10% of the thickness of the polycrystalline silicon semiconductor layer, the positions of the peaks being with respect to a surface of the substrate.* Such a structurally characterizing aspect of the thin film transistors of the LCD device, applicants submit, could not have been realizable even from the combined teachings of the above-named references.

In the case where a diffusion process is employed for effecting doping of a semiconductor, the highest impurity concentration is nearest the surface of the semiconductor. However, in the case where a conductivity type of a semiconductor is determined by employing an implantation process for the doping of the semiconductor, as in the case of the present invention, the highest impurity concentration is found at a distance inwardly from the surface of the semiconductor and, moreover, its depth distribution of concentration of the impurity is nearly Gaussian due to the statistical nature associated with the impurity stopping process.

Attached hereto is Sketch 1 for purposes of facilitating a better understanding of the following recitation of the above-noted featured aspect of the invention, contained in claims 1 and 5:

> variations of positions of peaks of depth distributions of concentration of impurities introduced into the polycrystalline silicon semiconductor layer by implantation.

Sketch 1 represents a schematic perspective view illustrating variations of positions of peaks of depth distributions of concentration of impurities introduced into the polycrystalline silicon semiconductor layer (crystallized by laser annealing) by implantation in connection with Figs. 4A and 4B of the drawings of the present application.

It is submitted, none of the above-named references disclosed or, for that matter, suggested, even when considered in combination, the just noted featured aspect of the invention. For example, it is admitted in the rejection (on page 3 of the Office Action) that "the reference [Yamazaki et al] lacks the unevenness of a surface of said polycrystalline silicon semiconductor layer being within 10% of the thickness of said polycrystalline silicon semiconductor layer," and, moreover, that Yamazaki et

al lacks the above-recited featured aspect of the invention, namely, that variations of positions of peaks of depth distributions of concentration of impurities introduced into the polycrystalline silicon semiconductor layer [by implantation] to determine a conductivity type thereof being within 10% of the thickness of the polycrystalline silicon semiconductor layer, the positions of the peaks being with respect to a surface of the substrate.

It is also stated in the Office Action that "Shimizu et al discloses the same method of making [applicants'] device wherein variations of positions of peaks of depth distributions of concentration of impurities introduced into the polycrystalline silicon semiconductor layer by implantation to determine the conductivity type thereof being within 10% of the thickness of the polycrystalline silicon semiconductor layer; the positions of the peaks being with respect to a surface of the substrate" (see the first full paragraph on page 5 of the Official Action). As will be shown below, however, the technique taught by Shimizu et al is clearly not the same as that which would be required for achieving the present invention.

Shimizu et al, it is submitted, did not disclose achieving doping of the polycrystalline silicon semiconductor layer by implantation of impurities. And, therefore, Shimizu et al did not disclose that the highest impurity concentration of a dopant occurs at a distance away from the surface of the polycrystalline silicon semiconductor layer. This is also supported by the above discussion and the showings in attached Sketch 1, which is illustrative of variations of positions of peaks of depth distributions of concentration of impurities that are introduced into the polycrystalline silicon semiconductor layer by the implantation process such as discussed in the specification with regard to Figs. 4A and 4B. Shimizu et al make no

reference to the polycrystalline silicon semiconductor layer being crystallized by laser annealing. According to Shimizu et al, the technique employed for obtaining a polycrystalline silicon film is by annealing and crystallizing an amorphous silicon film that is deposited on a silicon oxide film which serves as a substrate.

In the rejection it is stated that "Shimizu et al discloses (column 2, lines 25-45) the surface of the PS-a is exposed to hydrogen fluoride and then amorphous silicon film is deposited, annealed and crystallized therefore forming good film uniformity." (The second full paragraph on page 5 thereof.) According to Shimizu et al, however, the surface which is exposed to hydrogen fluoride treatment is not the surface of the polycrystalline silicon semiconductor film but, rather, it is the surface of the silicon oxide film serving as the substrate (see column 2, lines 38-45, and line 65, *et seq.*), which is in clear contradistinction with that alleged in the rejection. Namely, according to Shimizu et al, the silicon oxide film serving as a substrate is rinsed with an etching liquid, such as hydrogen fluoride, before the deposition of the amorphous silicon film on the silicon oxide film, in order to achieve a larger crystal grain diameter and good uniformity in the film thickness. On the other hand, as correctly noted by the Examiner, in which he cites the description on page 40, line 17 to page 42, line 11 (this portion is referred to as specification paragraphs [0111-0115] in the Office Action), the example technique employed by the present inventors call for exposing of the surface of the polycrystalline silicon semiconductor film PS-a to hydrogen fluoride, which is quite different than Shimizu et al's technique. Applicants submit, therefore, that it is erroneous to assume that Shimizu et al, allegedly, "discloses the same method of making the....device wherein variations of the positions of peaks of distributions of concentration of impurities introduced...by

implantation...being within 10% of the thickness of the polycrystalline silicon semiconductor layer..." (the first full paragraph on page 5 of the Office Action).

It is alleged in the Official Action that the device performance is improved by keeping the surface smooth (see the paragraph bridging pages 5 and 6 of the Official Action). For example, it is alleged in the rejection that, according to Takehashi et al, the roughness of the surface should be kept to a few nm (see the Abstract), which is therefore less than 10% when the layer thickness is 100 nm. (Such a thickness is mentioned in column 4, line 11, and in column 6, line 20, in Takahashi et al.) It is submitted, however, that Takehashi et al neither disclosed nor suggested the above-discussed featured aspect according to independent claims 1 and 5, namely, that:

> variations of positions of peaks of depth distributions of concentration of impurities introduced into the polycrystalline silicon semiconductor layer, crystallized by laser annealing, by implantation to determine a conductivity type thereof are within 10% of the thickness of the polycrystalline silicon semiconductor layer, the positions of the peaks being with respect to a surface of the substrate.

Regarding the teachings in Hasegawa, it is alleged in the rejection that "the surface should be smooth (as possible-abstract, and less than 10 angstroms in spec) and that enables the ability to control doping depth (col. 6, lines 30-49)." It is submitted, however, in Hasegawa <u>there is only disclosed a technique for obtaining a smooth flat surface by controlling the power applied for effecting plasma generation</u> (see col. 7). <u>Hasegawa neither disclosed nor suggested the crystallization by laser annealing</u> such as recited according to claims 1 and 5, which call for "a polycrystalline silicon semiconductor layer crystallized by laser annealing" in conjunction with the other recited aspects. Therefore, since Hasegawa make no reference to crystallization by laser annealing, unlike the present application, one of

ordinary skill would, therefore, not have been led to combine the teachings of Hasegawa with Yamazaki et al.

Although it is alleged in the rejection that Hasegawa's teachings enables the ability to control the doping depth, using as a basis the discussion in column 6, lines 30-49 thereof, such control, however, has a very limiting application. That is, Hasegawa's disclosure, it is submitted, is applicable only to a particular case where a polycrystalline silicon (poly-Si) film is formed of a two layer structure consisting of a <100> film and <110> film and a thermal diffusion is employed for the poly-Si film. As discussed earlier in these remarks, with regard to the attached Sketch 1, the depth distribution of concentration of the impurity for implantation as in the case of the present invention, is quite different from that as a result of thermal diffusion, as in the case of Hasegawa. Therefore, for at least the above reasons, Hasegawa's teachings are inapplicable to a configured scheme as that presently set forth. To further highlight this, it is noted that Hasegawa makes no reference to positions of peaks of depth distributions of concentration of conductivity-type-determining impurities introduced into the polycrystalline silicon semiconductor layer. Also, it is submitted, Hasegawa makes no reference to the thickness of the poly-Si film. Therefore, one of ordinary skill in this area of technology could not have conceived of a LCD device in which the thin film transistors are schemed such that **variations of positions of peaks of depth distributions of concentration of impurities introduced into the polycrystalline silicon semiconductor layer, crystallized by laser annealing, by implantation to determine a conductivity type thereof being within 10% of the thickness of the polycrystalline silicon semiconductor layer, the positions of the peaks being with respect to a surface of the substrate.**

This deficiency insofar as claims 1+ and 5+ are concerned, is also likewise the case regarding the teachings in Ipri.

In the rejection, it is also alleged that, according to Ipri, creating a smooth surface is desirable, and, according to the Examiner, leads to "good device properties". However, as alluded to hereinabove, Ipri also makes no reference to *positions of peaks of depth distributions of concentration of conductivity-type-determining impurities introduced into the polycrystalline silicon semiconductor layer.*

It is alleged also, that according to Yamazaki et al, "it would have been obvious...to retain as smooth a surface as possible (including within 100/c or better) for the purpose of better device properties as taught in any of the three secondary references" (see the sentence bridging pages 5 and 6 in the Office Action). The Examiner's assertion notwithstanding, and as was shown hereinabove, the characterizing control parameter directed to the thin film transistors of the schemed LCD device was clearly not taught by any of the applied references in the rejection nor could have been realizable even in view of their combined teachings. According to this featured control parameter, **variations of positions of peaks of depth distributions of concentration of impurities introduced into the polycrystalline silicon semiconductor layer, crystallized by laser annealing, by implantation to determine a conductivity type thereof by selecting the variations of positions of peaks of depth distributions of concentrations of impurities are within 10% of the thickness of the polycrystalline silicon semiconductor layer, the positions of the peaks being with respect to a surface of the substrate.** As was noted earlier in these Remarks, also, this schemed control parameter could not have been rendered obvious in the manner as that alleged in outstanding rejection,

especially since neither Yamazaki et al, Shimizu et al, Hasegawa, Takehashi et al or Ipri disclosed or suggested, either separately or even in combination, the utilization of the *variations of positions of peaks of depth distributions of concentrations of impurities* for controlling the performances of a liquid crystal display device. For example, as was shown by the above discussion regarding Yamazaki et al and Shimizu et al, in conjunction with the showings of Sketch 1 and related Figs. 4A and 4B of the present application, the concept of controlling variations of positions of peaks of depth distributions of concentration of impurities introduced into the polycrystalline silicon semiconductor layer by implantation could not have been suggested even from the combined teachings of Yamazaki et al. Accordingly, the invention as defined in claims 1 and 5 and, correspondingly, also according to the dependent claims 2 and 6 thereof, respectively, could not have been rendered obvious over the teachings of the cited references.

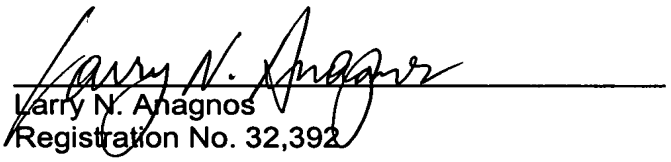
Therefore, for at least the above reasons, withdrawal of the outstanding art rejection and early allowance of the above-identified application is respectfully requested.

If the Examiner deems that questions and/or issues still remain which would prevent the present application from being allowed at the present time, she is urgently invited to telephone the undersigned representative, at the number indicated below, so that either a telephone or personal interview may be arranged at the Examiner's convenience in order to discuss the same and hopefully resolve any remaining questions/issues present.

To the extent necessary, applicants petition for an extension of time under 37 C.F.R. §1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including Extension of Time fees, to the Deposit Account of Antonelli, Terry, Stout & Kraus, LLP, Dep. Acct. No. 01-2135 (520.39294CX1), and please credit any excess fees to such deposit account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP.



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